

**S/N Unknown**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Biswajit Sur et al.	Examiner:	Unknown
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	Herewith	Docket:	884.319US2
Title:	ELECTRONIC ASSEMBLY COMPRISING SOLDERABLE THERMAL INTERFACE AND METHODS OF MANUFACTURE		
Assignee:	Intel Corporation	Customer No:	21186

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**INFORMATION DISCLOSURE STATEMENT**

MS Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Pursuant to 37 C.F.R. §1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicants' prior U.S. application, Serial No. 09/652430, filed on August 31, 2000, which is relied upon for an earlier filing date under 35 U.S.C. §120.

INFORMATION DISCLOSURE STATEMENT

Serial No :Unknown

Filing Date: Herewith

Title: ELECTRONIC ASSEMBLY COMPRISING SOLDERABLE THERMAL INTERFACE AND METHODS OF MANUFACTURE

Assignee: Intel Corporation

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Dkt: 884.319US2 (INTEL)

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

BISWAJIT SUR ET AL.

By their Representatives,

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Date Feb 6, 2004

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Date of Deposit: February 9, 2004

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.

Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)	<i>Complete if Known</i>	
	<b>Application Number</b>	Unknown
	<b>Filing Date</b>	Even Date Herewith
	<b>First Named Inventor</b>	Sur, Biswajit
	<b>Group Art Unit</b>	Unknown
	<b>Examiner Name</b>	Unknown
Sheet 1 of 1		Attorney Docket No: 884.319US2

US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-4,561,011	12/24/1985	Kohara, Masanobu, et al.	356	81	09/22/1983
	US-4,827,376	05/02/1989	Voss, Scott V.	361	388	12/18/1987
	US-5,098,609	03/24/1992	Iruvanti, S., et al.	252	511	11/03/1989
	US-5,276,289	01/04/1994	Satoh, R., et al.	174	260	03/25/1991
	US-5,396,403	03/07/1995	Patel, C.	361	705	07/06/1993
	US-5,587,882	12/24/1996	Patel, C.	361	705	08/30/1995
	US-5,623,394	04/22/1997	Sherif, R. A., et al.	361	705	08/02/1996
	US-5,672,548	09/30/1997	Culnane, T. M., et al.	437	209	06/26/1996
	US-5,744,863	04/28/1998	Culnane, T. M., et al.	257	712	06/07/1995
	US-5,880,524	03/09/1999	Xie, Hong	257	704	05/05/1997
	US-5,905,636	05/18/1999	Baska, D. A., et al.	361	705	01/23/1998
	US-6,091,603	07/18/2000	Daves, Glenn G., et al.	361	704	09/30/1999
	US-6,218,730	04/17/2001	Toy, Hilton T., et al.	257	704	01/06/1999
	US-6,281,573	08/28/2001	Atwood, E. R., et al.	257	706	03/31/1998
	US-6,292,369	09/18/2001	Daves, Glenn G., et al.	361	719	08/07/2000
	US-6,294,408	09/25/2001	Edwards, David L., et al.	438	121	09/30/1999
	US-6,372,337	04/16/2002	Takahashi, Takayuki, et al.	428	328	05/26/1999

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
	JP-03142860	06/18/1991	Tetsuya, H.	H01L	23/02	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		AMENDOLA, A., et al., "Cooling Structure for an Integrated Circuit Module", IBM Technical Disclosure Bulletin, Vol. 23, No. 2, XP002191051, (July 1980),602	
		HAYASHIDA, TETSUYA, "Manufacture of Semiconductor integrated circuit device", Patent Abstracts of Japan, Vol. 015, No. 365 (E-1111), (09 13 1991),	
		MILLER, R. C., "Structure for achieving thermal enhancement in a semiconductor package", IBM Technical Disclosure Bulletin, Vol. 23, No. 6, XP002191052, (Nov 1980),2308	

EXAMINER

DATE CONSIDERED